Notice of Allowability	Application No.	Applicant(s)	
	10/028,300	YOO ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed October 11, 2006*.

2. ☒ The allowed claim(s) is/are *1,2,5-7,9,11-14 and 17-31*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) None
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 11, 2006 has been entered.

Accordingly, claim 1 was amended, and claims 3, 4, 8, 10, 15 and 16 were cancelled. Currently, claims 1, 2, 5-7, 9, 11-14 and 17-31 are pending in this application.

Allowable Subject Matter

2. Claims 1, 2, 5-7, 9, 11-14 and 17-31 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claim 1, none of the prior art of record discloses, inter alia, a liquid crystal display device comprising:

a gate insulating film entirely covering the gate line wherein the data line is disposed on the gate insulating film, and wherein the gate line is disposed directly on a substrate;

a storage electrode sunken in the gate insulating film to overlap with the gate line, said storage electrode uncovered by and disposed upon said gate insulating film; and

a protective layer on the gate insulating film to cover the data line, the gate line and the thin film transistor,

wherein a contact hole passes through the protective layer and a portion of the gate insulating film having the storage electrode sunken therein, the pixel electrode is connected to the storage electrode via the contact hole, and the gate insulating film contacts a vertical side surface of the storage electrode.

The most relevant reference, US 6,356,318 B1 to Kawahata, fails to disclose or suggest the gate insulating film contacts a vertical side surface of the storage electrode. As shown in Fig. 1, Kawahata discloses a gate insulating film 8, 10 entirely covering the gate line 7 wherein the data line 13 is disposed on the gate insulating film 8, 10, and wherein the gate line 7 is disposed directly on a substrate 1;

a storage electrode 15 sunken in the gate insulating film 8, 10 to overlap with the gate line 7', said storage electrode uncovered by and disposed upon said gate insulating film 8, 10; and

a protective layer 16 on the gate insulating film 8, 10 to cover the data line 13, the gate line 7 and the thin film transistor 11,

wherein a contact hole 18 passes through the protective layer 16 and a portion of the gate insulating film 8 having the storage electrode sunken therein, the pixel electrode 19 is connected to the storage electrode 15 via the contact hole 18.

However, the gate insulating film 10 does not contact a vertical side surface of the storage electrode 15; instead, the gate insulating film 10 contacts the bottom surface of the storage electrode 15.

Re claims 5 and 17, none of the prior art of record discloses, in combination with other limitations as claimed, a method of fabricating a liquid crystal display having a storage electrode comprising:

forming a gate line and a gate electrode of a thin film transistor on a substrate;

depositing a first gate insulating film on the substrate to cover the gate electrode and the gate line;

forming the storage electrode on a first gate insulating film to overlap with the gate line disposed directly on the substrate;

depositing a second gate insulating film on the first gate insulating film to cover the storage electrode;

forming an active layer and an ohmic contact layer on the gate insulating films;

forming a source electrode and a drain electrode on the ohmic contact layer;

forming a protective layer on the gate insulating films to cover the source electrode and the drain electrode; and

forming a pixel electrode connected to the drain electrode.

The most relevant reference, USPN 6,356,318 B1 to Kawahata, fails to disclose or suggest the claimed invention.

As shown in Figs. 1 and 5, Kawahata discloses a first gate insulating film 8 and a second gate insulating 10 deposited on the first gate insulating 8; however, the storage electrode 15 is formed on top of the second gate insulating layer 10. Meanwhile, Fig. 3 of Kawahara shows that the second gate insulating film 10 is formed on the first gate insulating film 8 to cover the storage electrode 15; however, the active layer 12, the

source electrode and the drain electrode are not formed on the second gate insulating layer 10.

Finally, re claim 7, Fig. 1 of Kawahara does not show that a first contact hole 18 passes through the protective layer 16 and a portion of the second gate insulating film 10 having the storage electrode 15 formed on the first gate insulating film 8 since the storage electrode 15 is formed on top of the second insulating film 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

DUNG T. NGUYEN
PRIMARY EXAMINER

Thoi Duong

12/05/2006